REMARKS

Claims 1-3 and 10 were rejected. Claims 4-9 and 11-14 were objected to. Claims 15 and 34-46 were allowed. With this response, new claims 47-56 are added, no new matter is present in those claims, and the examiner has previously indicated that the subject matter is allowable. With this response, claims 1, 3, 6, 7, 9, 10, and 12-14 are amended, no new matter is added. Claims 1-15 and 34-56 remain pending. Reconsideration of claims 1-14 and allowance of claims 1-14 and 47-56 is respectfully requested in view of the following remarks.

Claim Objections

Claims 3 and 10 were objected to because the term "data IO lines" found in claims 3 and 10 is not consistent with "common data IO lines" as defined in claim 1. The applicant has overcome this objection by removing the term "common data IO lines" from claim 1, replacing it with the limitation "a first and a second data IO line, wherein the second data IO line is complementary to the first data IO line." Support for this amendment can be found in the original disclosure (FIG. 6; page 1, lines 12-13; claims 4 and 7). The amendment to claim 1 required that claims 3, 6, 7, 9, 10, and 12-14 be amended as well to keep the claim language consistent throughout.

Claim Rejections – 35 USC § 102

Claims 1-3, 10 were rejected under 35 U.S.C. 102(b) as being anticipated by Sato et al. (U.S. Patent No. 5,065,363). The applicant respectfully disagrees for the following reason.

Amended claim 1 recites, in part, "the read charge control circuit and the write charge control circuit both coupled to a first and a second data IO line, wherein the second data IO line is complementary to the first data IO line." Contrary to the recited limitation, Sato states that, with regard to FIG. 1, "[i]n the present embodiment, the data lines for writing and the data lines for reading are ***not*** arranged in the form of complementary data lines." (column 4, lines 31-33, emphasis added).

With regard to Sato's FIG. 8, there is disclosed a first data line Dwq and a second data line Drq (column 20, lines 49-50). If MOSFETs Q55 and Q54 in Sato FIG. 8 are a read charge control circuit and a write charge control circuit, respectively, then they are not each coupled to the first data line (Dwq) and the second data line (Drq). Furthermore, Sato does

not disclose that Dwq and Dwr are complementary to each other. Thus, Sato's "read charge control circuit" (Q55, FIG. 8) and "write charge control circuit" (Q54, FIG. 8) are not both coupled to a first data line and a second data line that is complementary to the first data line.

The applicant believes that claims 2, 3, and 10 are also not anticipated by Sato for at least the same reason as claim 1.

Allowable Subject Matter

Claims 4-9 and 11-14 were objected to as being dependent upon a rejected base claim, but the examiner indicated that they would be allowable if rewritten in independent form to include all the limitations of the base claim and any intervening claims.

The applicant adopts this suggestion with the addition of new claims 47-56 (10 claims). New independent claims 47, 50, 53, and 54 contain the limitations of claims 1 and 4; claims 1 and 7; claims 1, 10 and 11; and claims 1 and 12, respectively. New dependent claims 48, 49, 51, 52, 55, and 56 are modeled after claims 5, 6, 8, 9, 13, and 14, respectively, but depend upon the appropriate new independent claim, and thus are also in condition for allowance.

Conclusion

For the foregoing reasons, reconsideration of claims 1-14 and allowance of claims 1-14 and 47-56 of the application as amended is solicited. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

1. (Twice Amended) A circuit, comprising:

a read charge control circuit activated only during read operations by a read signal and an address; and

a write charge control circuit activated by a write signal and the same or a different address, the read charge control circuit and the write charge control circuit both coupled to [common] a first and a second data IO [lines] line, wherein the second data IO line is complementary to the first data IO line.

3. (Twice Amended) The circuit according to claim 1 wherein the write charge control circuit transfers charge between at least one of the first and second data IO lines and a bit [lines] line.

6. (Twice Amended) The circuit according to claim 4 wherein the first write controlled gate is coupled directly between the bit line and [a] the first data IO line and the second write controlled gate is coupled directly between the complementary bit line and [a complementary] the second data IO line.

7. (Twice Amended) The circuit according to claim 1 wherein the read charge control circuit includes a first read controlled gate controlling charge from a bit line to [a complementary] the second data IO line and a second read controlled gate controlling charge from a complementary bit line to [a] the first data IO line.

9. (Twice Amended) The circuit according to claim 7 wherein the first read controlled gate is coupled directly between the bit line and the [complementary] second data IO line and the second read controlled gate is coupled directly between the complementary bit line and the first data IO line.

10. (Twice Amended) The circuit according to claim 1 including a data output sense amplifier coupled between a data output buffer and the first and second data IO lines.

12. (Twice Amended) The circuit according to claim 1 wherein the read charge control circuit includes:

a first transistor having a first terminal coupled to a bit line, a second terminal coupled to [a complementary] the second data IO line, and a third terminal;

a second transistor having a first terminal coupled to a complementary bit line, a second terminal coupled to [a] the first data IO line, and a third terminal; and

a third transistor having a first terminal coupled to a column select line, a second terminal coupled to the third terminal of the first and second transistor, and a third terminal coupled to a first reference voltage.

13. (Twice Amended) The circuit according to claim 12 wherein the write charge control circuit includes:

a first transistor having a first terminal coupled to a write column select line, a second terminal coupled to the complementary bit line, and a third terminal coupled to the [complementary] second data IO line; and

a second transistor having a first terminal coupled to the write column select line, a second terminal coupled to the first data IO line, and a third terminal coupled to the bit line.

14. (Twice Amended) The circuit according to claim 13, [including] further comprising:

a first load transistor having a first terminal coupled to a second reference voltage, a second terminal coupled to the first data IO line, and a third terminal coupled to a third reference voltage; and

a second load transistor having a first terminal coupled to the second reference voltage, a second terminal coupled to the [complementary] second data IO line, and a third terminal coupled to the third reference voltage.

Claims 47-56 are new.